A Monolithic 75–110 GHz Balanced InP-Based HEMT Amplifier

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***Abstract*—A monolithic balanced amplifier covering the entire W-band (75–110 GHz) have been developed using 0.1-μm pseudomorphic InAlAs–InGaAs–InP HEMT technology. This MMIC amplifier demonstrated first pass success with a measured gain of 23 ± 3 dB and good return loss from 75 to 110 GHz. The noise figure of this amplifier is about 6 dB around 94 GHz. To our knowledge, this is the best reported broad-band and high gain performance of the monolithic amplifiers covering the entire W-band.**

I. Introduction

W-BAND (75–110 GHz) low-noise amplifiers (LNA's) are important components for test equipment, radar, and passive imaging applications. Development of monolithic W-band LNA's has been reported using various device technologies, including GaAs-based MESFET's [1], GaAs-based HEMT's [1]–[7], and InP-based HEMT's [8]–[11]. Among the existing device technologies, InP-based HEMT's have demonstrated the best gain and low noise performance on a discrete device level [12]–[13], since the InAlAs–InGaAs–InP material system exhibits high mobility and peak velocity and a large bandgap discontinuity between the InAlAs and InGaAs layers. These lead to higher device gain, higher cutoff frequency, lower noise figure and lower dc power consumption compared with GaAs-based material systems.

Wide-band monolithic InP HEMT amplifiers have been reported using distributed amplifier approaches [9]–[10] with 5–6 dB at W-band. The motivation of this work is to construct a high gain monolithic multistage amplifier using InP-based HEMT's covering the entire W-band. This letter reports a monolithic balanced amplifier covering the entire W-band using 0.1 μm InP based HEMT technology. This amplifier demonstrated a measured gain of 23 ± 3 dB from 75 to 110 GHz with good return loss, which is the best reported broad-band and high gain performance of the monolithic amplifiers at W-band.

II. Device Fabrication and Characteristics

The InAlAs–InGaAs–InP HEMT structure shown in Fig. 1 is similar to that reported before [11], [13]. The high quality InP HEMT structure is grown using molecular beam epitaxy on a two-inch Fe-doped substrate. The typical room temperature and 77 K mobilities are 10 500 and 35 000 cm^2/V-sec, respectively, with a sheet carrier concentration typically between 3.0–3.5×10^{12} cm^{-2}. Silicon planar doping is employed in the InAlAs layer to simultaneously achieve a high channel aspect ratio for a 0.1-μm gate length device and high electron transfer efficiency. Doping levels and layer thicknesses are optimized to achieve sharp pinch off characteristics, high transconductance levels and good Schottky characteristics. The device structure and layout are also carefully designed to yield minimum parasitic capacitances and resistances. All of these parameters have been found to impact the minimum noise figure of the device.

This 0.1-μm gate length pseudomorphic (PM) InP HEMT's ($In_{0.6}$ $Ga_{0.4}$ As channel) have achieved state-of-the-art performance with a dc transconductance of 1300 mS/mm, a unit current gain cutoff frequency (f_T) of 240 GHz, and an extrapolated maximum oscillation frequency (f_{max}) of 400 GHz. The typical gate leakage current is around 5 μA and the gate-to-drain breakdown voltage is 2–2.5 V. The high value of gate leakage current is mainly due to the planar boron in-implantation process used for device isolation. A measured noise figure of 1.3 dB at 95 GHz with an associated gain of 8.2 dB, and a measured gain of 7.3 dB at 140 GHz were obtained for single-stage hybrid amplifiers using InP HEMT devices [13]. The same device also achieved state-of-the-art performance for a Q-band hybrid cryogenically cooled amplifier which demonstrated a noise temperature of 13 K at 41 GHz [14].

The InP HEMT MMIC fabrication process was adopted from the baseline MMIC fabrication process used for GaAs-based HEMT MMIC's [3]–[5]. The differences in the fabrication process steps include the device isolation process, the ohmic metallization, alloying conditions and the through substrate via hole etch. The MMIC LNA's fabricated using this process have also achieved state-of-the-art high gain and low-noise figure performance at lower frequencies, which include a Q-band (44 GHz) two-stage LNA exhibiting 2.2-dB noise figure with 25-dB associated gain [15] and a V-band three-stage LNA demonstrating less than 3-dB noise figure with 24-dB gain at 60 GHz [16].

III. Circuit Design and Performance

The HEMT linear small signal equivalent circuit parameters are obtained from careful fit of the measured small signal S-parameters to 40 GHz. The noise model parameters are obtained from fitting measured noise parameters to 26 GHz. These parameters are consistent with an estimation based

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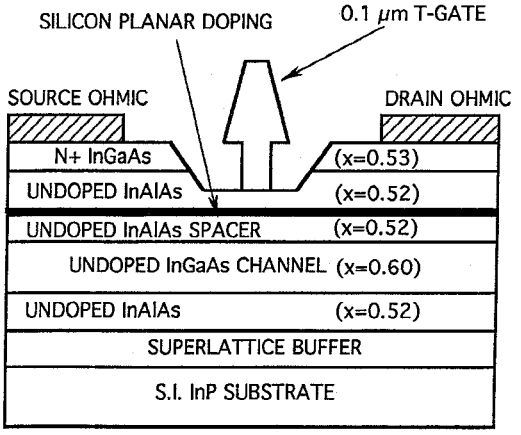
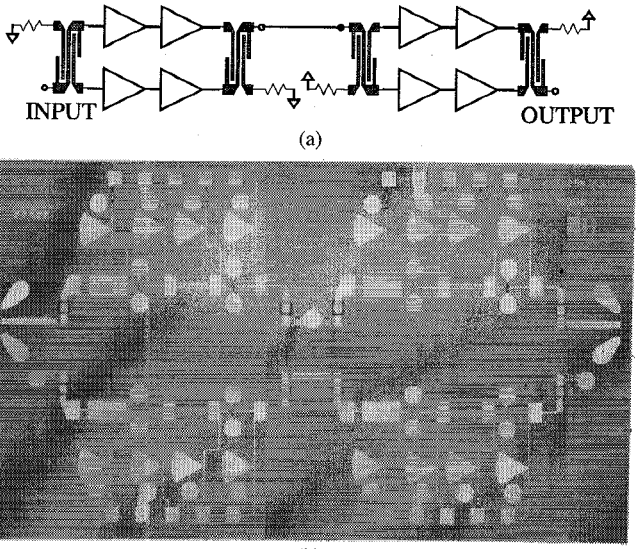


Fig. 1. The device profile of the 0.1-μm PM InAlAs–InGaAs–InP HEMT device.



(a)

(b)

Fig. 2. (a) The circuit block diagram, and (b) the photograph, of the monolithic W-band four-stage blanced InP HEMT amplifier.

on device physical dimensions and parameters. The device modeling and circuit design procedures were described in [3].

Fig. 2(a) and (b) show the block schematic diagram and the monolithic chip photograph. The size of the chip is 4.2 × 2.4 mm^2. The balanced amplifier is a four-stage design, which is formed by cascading two identical two-stage balanced gain stage using four-finger Lange couplers. Each stage utilizes a four-finger HEMT with 40-μm total gate periphery. This approach provides good return loss over wide bandwidth and better amplifier stability. However, the gain was traded off by using multiple Lange couplers. The matching networks in the gain stage are designed for high gain over wide bandwidth and constructed by cascading high-low impedance microstrip lines. Edge coupled lines are used for dc blocking and radial stubs are employed for RF bypass. Shunt n^+ bulk resistors are used in the bias networks for amplifier stability. A wet chemical etching process is used to fabricate back side via holes through the InP substrated for grounding.

The monolithic balanced amplifier was measured at a verified W-band on-wafer probe test set [17]. The measured small

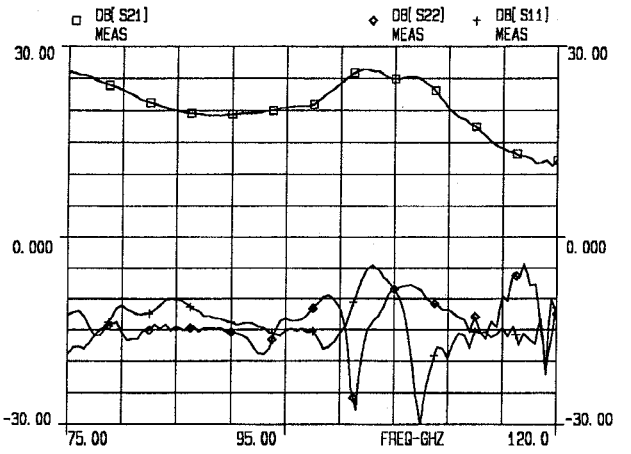


Fig. 3. Measured small signal gain and return loss of the monolithic W-band four-stage balanced InP HEMT amplifier from 75 to 120 GHz.

signal gain and return loss from 75 to 120 GHz are plotted in Fig. 3. The amplifier demonstrated a measured gain of 23 ± 3 dB from 75 to 110 GHz with input and output return loss greater than 10 dB for most of the frequencies. The data was taken at a drain voltage of 0.9 V and a drain current of 19 mA for each stage. Since there is a 100 Ω shunt resistor in each drain bias network which draws 9-mA current at a 0.9-V drain voltage, the current drawn by each transistor is about 10 mA. A two-stage balanced gain stage was fabricated on the same wafer, which exhibits a measured noise figure of 6 dB around 94 GHz. Thus the noise figure of the complete four-stage balanced amplifier is estimated to be 6–6.5 dB. The design goal of this amplifier was to achieve 24 ± 3 dB gain from 75 to 110 GHz while the simulation results showed 24 ± 1 dB gain across the band. The measured data (23 ± 3 dB) is close to the design goal but presents a higher gain ripple compared with the simulated results. One possible reason for the discrepancy is that we failed to analyze the interactions among entire structures owing to the limitation of existing full-wave EM analysis tools, although each individual passive component in the circuit was modeled via EM analysis.

IV. Summary

We have demonstrated a first-pass-success monolithic balanced W-band amplifier based on 0.1 μm PM InAlAs–InGaAs–InP HEMT's. A small signal gain of 23 ± 3 dB with good return loss from 75 to 110 GHz was achieved. This is the best broad band and high gain performance of the monolithic amplifiers for the entire W-band.

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